- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3.2V-50V
- Low Shutdown Current 3.7μA
- Low Quiescent operating Current: 450μA
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dithering for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Supports additional Slope Compensation
- 22ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjust Under-Voltage Lockout
  - Constant Current Overload Protection
  - Thermal Shutdown Protection:165°C
- MSOP-8L(3mm*3mm) Package

- Muti-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

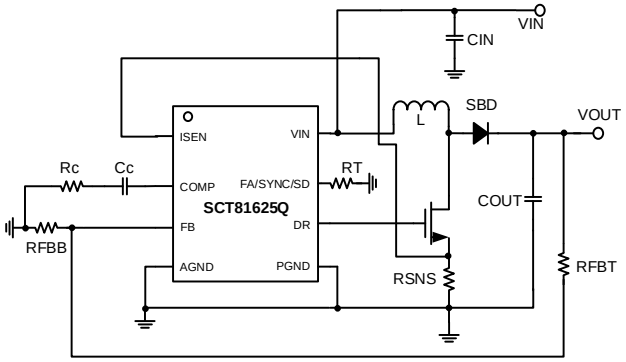
The SCT81625Q device is a wide input, non-synchronous boost controller. The Device can be used in Boost, SEPIC and Flyback converters and topologies.

The switching frequency of the SCT81625Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

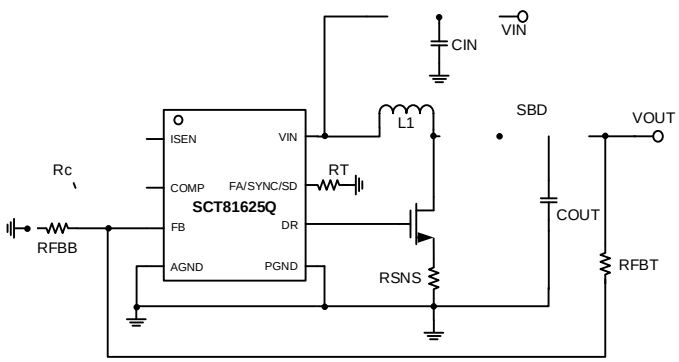
The SCT81625Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81625Q features Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81625Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.7μA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-8L(3mm*3mm) Package.



BOOST



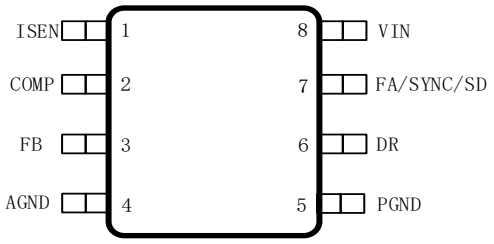
SEPIC

E6+ARXV _f SVcd WcacVgZfd cVgZdZ _d Rj UZdWcVd aRXV _f SVcd Z_eYV Tf cV_egVcdZ _ CVgZdZ _ +CV VRdVU e > Rc Ve

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT81625QMTDR	Tape & Reel	4000	1625Q	8	8-Lead 3mm×3mm Plastic MSOP

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	62	V
DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C



Top View: 8-Lead Plastic MSOP 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

NAME	NO.	DESCRIPTION
ISEN	1	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
COMP	2	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and GND.
FB	3	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1.26V typical.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
FA/SYNC/SD	7	Switching frequency setting pin. The switching frequency is programmed by a single resistor between this pin and AGND. The internal clock can be synchronized to an VieVc_R T T 2 YZXY VgV _eYZd aZ_Wc d h Z ef c_eYV UVgZTV WWR_UeYV device will then draw 3.7 µA from the supply typically.
VIN	8	Power supply input pin

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.2	50	V
V_{CC}	VCC voltage range	3.2	6.1	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

PARAMETER	THERMAL METRIC	MSOP-8	UNIT
$R_{\theta 2}$	Junction to ambient thermal resistance(1)	132.8	°C/W
$R_{\theta 4 (top)}$	Junction to case (top) thermal resistance(1)	64.1	°C/W
$R_{\theta B}$	Junction to board thermal resistance(1)	83.8	°C/W

(1) SCT provides $R_{\theta 2}$ and $R_{\theta 4}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta 2}$ and $R_{\theta 4}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81625Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81625Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta 2}$ and $R_{\theta 4}$.

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.92		50	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.9 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V		3.7	8	uA
I_Q	Quiescent current from VIN	no load, no switching		460		uA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.241	1.26	1.278	V
		Tj=-40~125°C	1.222		1.297	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	500	700	900	uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	120	155	195	uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	-170	-130		

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

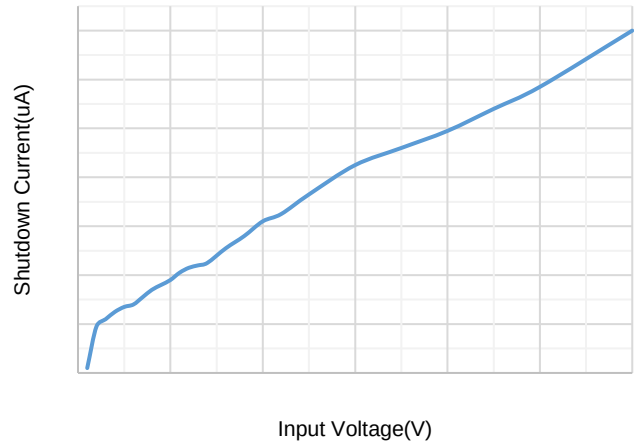


Figure 1. ISD vs Input Voltage

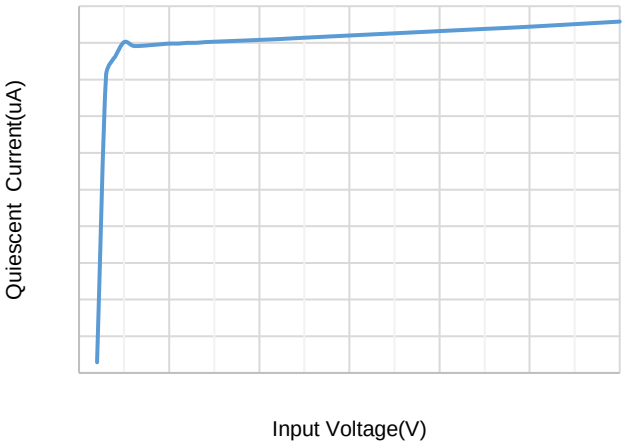


Figure 2. IQ vs Input Voltage

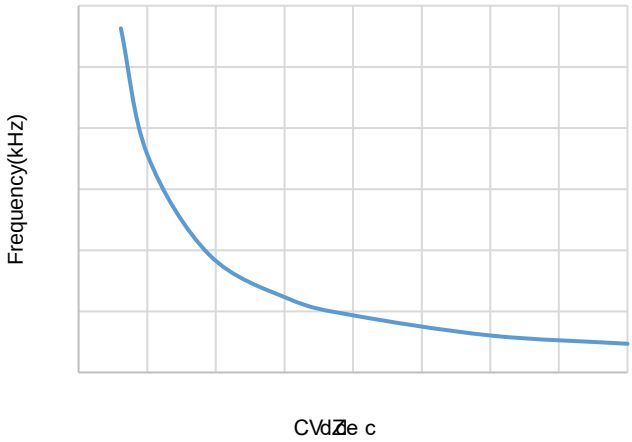


Figure 3. Switching Frequency vs RT

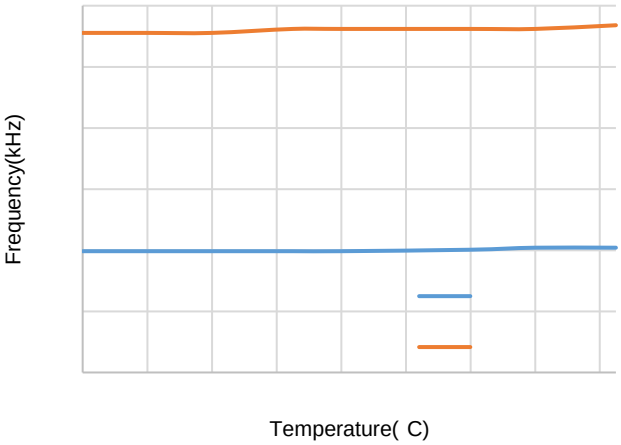


Figure 4. Switching Frequency vs Temperature

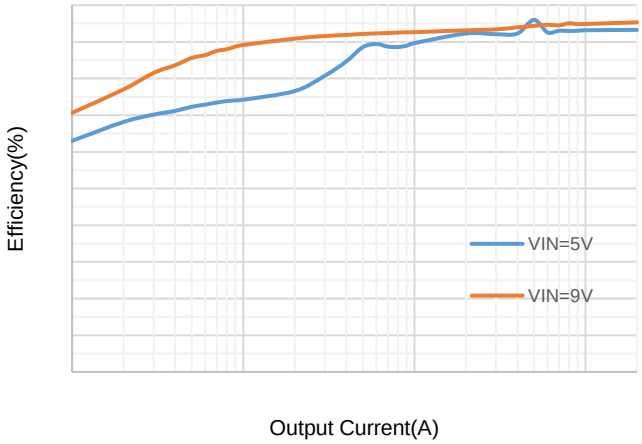


Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

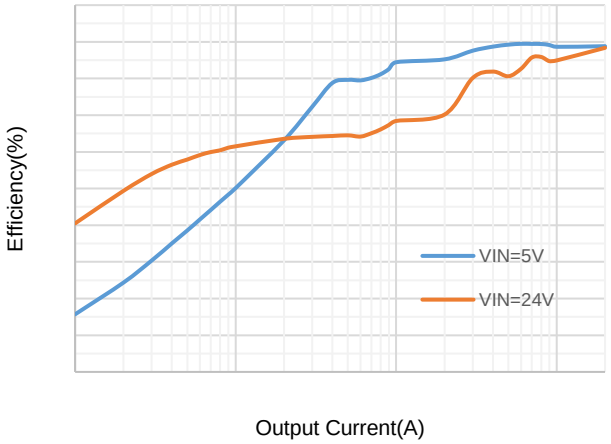


Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

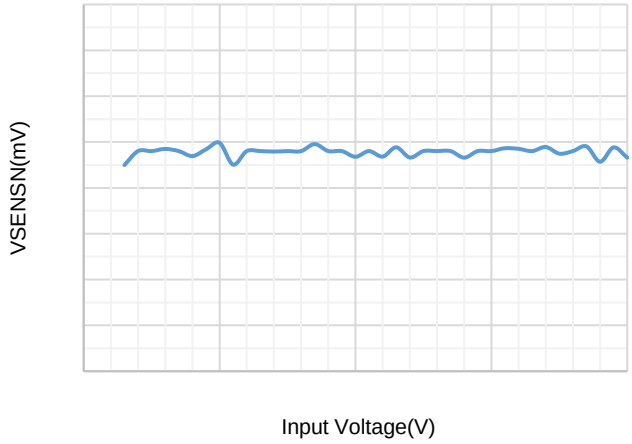


Figure 7. VSENSN vs Input Voltage

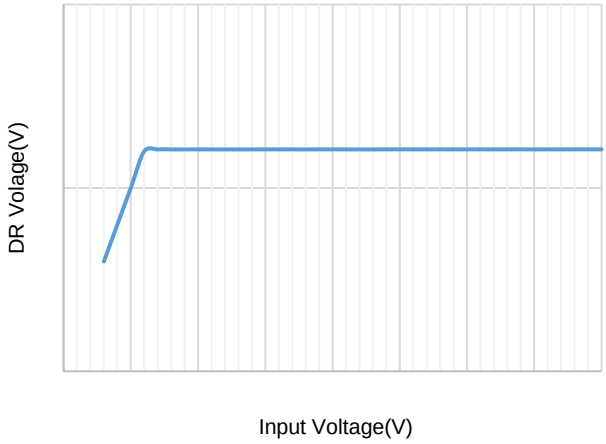


Figure 8. DR Volage vs Input Voltage

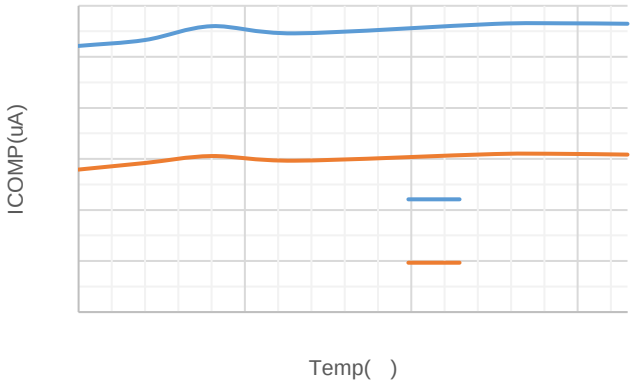


Figure 9. COMP Current vs Temperature

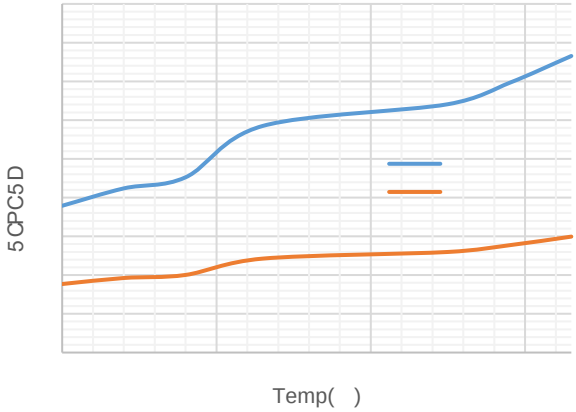


Figure 10. DR Resistance vs Temperature

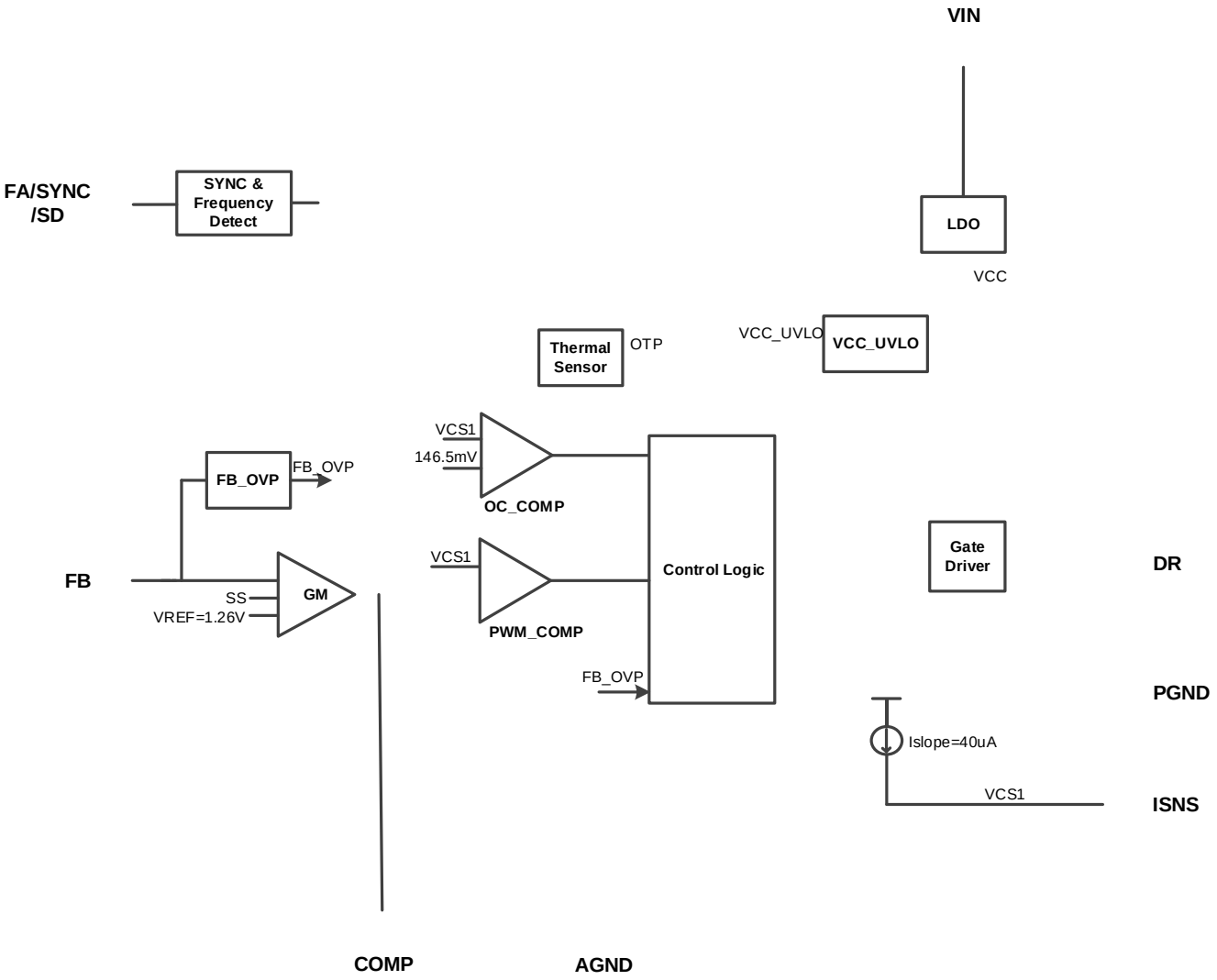


Figure 11. Functional Block Diagram

EYV Tf ccV_e UV T _ec dTYV VdR a Vd eYV Z_Uf Te c Tf ccV_e := R_U T aRcVd eYV dR a VU dZX_R GdR a e R Z_eVc_R j XV_VdReVU T _ec dZX_R GT EYV Tf ccV_e dV_dV cVdZde c CD6 Rd dY h _ Z_ 7ZXf cV T _gVcod eYV dR a VU Z_Uf Te c Tf ccV_e := e eYV g eRXV dZX_R GdR a eYReZd ac a ceZ_R e := df TY eYRe :

$$V_{samp} \quad I_L * R_{SEN} \tag{1}$$

7ZXf cV Zf de eRe V eYV eYV cj h Yj Df S 9 Rc _Zf dTZReZ_ YRaaV_ eYV cZdZ_X R_U WR Z_X d aVd > R_U > cVdaVTeZgVj WGdR a RcV R d ac a ceZ_R e eYV Z_Uf Te c Tf ccV_e cZdZ_X R_U WR Z_X d aVd > _ R_U > WW cVdaVTeZgVj H YVcV > _ Zd eYV Z_Uf Te cd aV Uf cZ_X eYV dh ZeTY _ eZ V R_U > WWZd eYV Z_Uf Te cd aV Uf cZ_X eYV dh ZeTY WWeZ V R_U RcV cVReVU e > R_U > Sj :

$$M_1 \quad M_{on} * R_{SEN} \tag{2}$$

$$M_2 \quad M_{off} * R_{SEN} \tag{3}$$

7 ceYV S dee a Xj +

$$M_1 \quad M_{on} * R_{SEN} \quad Vin * R_{SEN} / L \tag{4}$$

$$M_2 \quad M_{off} * R_{SEN} \quad (Vout \quad Vin) * R_{SEN} / L \tag{5}$$

:_ 7ZXf cV R d R Z_TcVRdV Z_ eYV RU Tf ccV_e TRf dVd eYV dR a VU dZX_R e Z_TcVRdV Sj GdR a EYV VWWTe W eYZd RU TYR_XV GdR a ReeYV V_U WeYV VZdedh ZeTYZ_X Tj T V Zd

$$'V_{samp1} \quad (\frac{M_2 \quad M_c}{M_1 \quad M_c}) * 'V_{samp0} \tag{6}$$

D H YV_ T aV_dReZ_dR a dZX_R ZdRUUVU h YZTY > T Zd Vc eYV_+

$$'V_{samp1} \quad (\frac{M_2}{M_1}) * 'V_{samp0} \quad (\frac{D}{1 \quad D}) * 'V_{samp0} \tag{7}$$

H YV_ 5 / & GdR a h Z SV XcVReVc eYR_ GdR a :_ eYVc h dUd eYV UZdef cSR_TV Zd UZgVcXV_e D RgVcj d R aVcef cSReZ_Z_eYV RU h Z TRf dV eYV UZdef cSR_TV e Z_TcVRdV

2 WWcR T aV_dReZ_dR a Zd RUUVU e eYV T _ec dZX_R E V_df cV eYRe eYV aVcef cSVU dZX_R T _gVcXVd h V f de RZ_eRZ_+

$$\left| (\frac{M_2 \quad M_c}{M_1 \quad M_c}) \right| < 1 \tag{8}$$

EYV T aV_dReZ_dR a YRd SVV_RUUVU Z_eVc_R j Z_eYV D4E) ' &B EYV d aV WeYZd T aV_dReZ_dR a YRd SVV_dV VTeVU e dReZdWV deRaa ZdReZ_d R_U Zd gRf VUVaV_Ud _eYV dh ZeTYZ_X WWbf V_Tj EYZd d aV TR_SV TR Tf ReVU f dZ_X eYV Wc f R+

$$M_c \quad V_{SL} * F_s \tag{9}$$

GD= Zd eYV R a Zef UV W eYV Z_eVc_R T aV_dReZ_dR a R_U 7D Zd eYV T _ec Vcd dh ZeTYZ_X WWbf V_Tj

7 c cV WWi ZSZZej d aV T aV_dReZ_TR_SV Z_TcVRdVU Sj RUUZ_X _V Vi eVc_R cVdZde c CD= Z_eYV :D6 d aReY 7ZXf cV dY h d eYV dVef a EYV Vi eVc_R j XV_VdReVU d aV T aV_dReZ_Zd eYV_RUUVU e eYV Z_eVc_R d aV T aV_dReZ_WeYV D4E) ' &B H YV_ f dZ_X Vi eVc_R d aV T aV_dReZ_eYV Wc f R Wc > T SVT Vd+

$$M_c \quad (V_{SL} \quad K * R_{SL}) * F_s \tag{10}$$

2 ej aZTR gRf V Wc VRTe c< Zd % 2

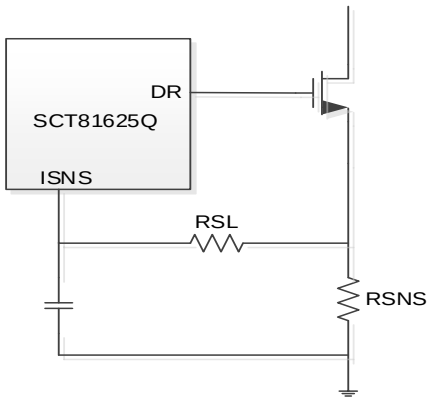


Figure13 .External RSL to increase slope compensation

Adjustable Peak Current Limit

EYV UVgZTV ac gZUVd Tj TV Sj Tj TV aVR Tf ccV_e Z Ze ac eVTeZ _ eYReef c_d WWeYV > D76E h YV_ eYV df WeYV Z_Uf Te c Tf ccV_eR_U eYV ac XdR RSVd aVT aV_dReZ _dR a cVRTYVd eYV Tf ccV_e Z ZeeYcVdY U AVR Z_Uf Te c Tf ccV_e Z Ze :A62< 4= Z_ deVRUj deReV Zd TR Tf ReVU Rd dY h _ Z_+

$$I_{PEAK\_CL} \quad \frac{V_{SENSE} \quad 40uA \ uR_{SL} \ uD}{R_{SNS}} \tag{11}$$

Where

- V_{SENSE} is ISEN pin limiting voltage (Typ.=146.5mV)
- $I_{PEAK-CL}$ is the inductor peak current limit
- R_{SL} is Slope compensation resistor
- D is Duty cycle
- R_{SNS} is the Inductance peak current detection resistance

H YV_ gVc RU YRaaV_d eYV T _gVceVc TR__ eac gZUV feafe Tf ccV_ee dReZdW RUZ_X cVbf ZcV V_e EYV Z_Uf Te c Tf ccV_eZd TR aVU Re gVc Tf ccV_e Z ZeReZ _ EYf d eYV feafeg eRXVUc ad SV h cVXf ReVU g eRXVh ZeY 73 g eRXV Vdd eYR_ Z_eVc_R cVWcV_TV g eRXV T _eZ_f f d j EYV Z_eVc_R 4 > A g eRXV cR ad f a e YZXY

3 VTRf dV 5 TR_ SV gRcZRS V f _UVcUZWcV_eGZ_ :A62< 4= Zd _ ede RS V f _UVcUZWcV_eGZ_ h YV_ f dZ_X Vi eVc_R d aV T aV_dReZ _ cVdZde c D Wc R_ RTTf dReV aVR Tf ccV_e Z Ze aVdReZ _ gVc eYV Z_af e df aa j g eRXV D4E cVT V_Ud f dZ_X _j eYV WZVU d aV T aV_dReZ _

Output Voltage

EYV feafeg eRXV Zd dVeSj R_ Vi eVc_R cVdZde cUZgZUVc C73E R_U C733 Z_ej aZTR Raa ZTReZ _dTYV ReZT 2 Z_Z f Tf ccV_e Wej aZTR f2 Wh Z_X eYc f XYWVUSRT cVdZde cUZgZUVc XZgVd X URTTf dRTj R_U _ ZdV T gVcZ_X EYV gR f V WC73E TR_ SV TR Tf ReVU Sj 6bf ReZ _

$$R_{FBT} \quad \frac{V_{OUT} \quad V_{REF}}{V_{REF}} \quad R_{FBB} \tag{12}$$

where:

- V_{REF} is the feedback reference voltage, typical 1.26V

Frequency Adjust/Shutdown/ Synchronization

EYV dh ZeTYZ_X WWbf V_Tj WeYV D4E) ' &B TR_ SV RU f deVU SVeh VV_ 9 R_U > 9 f dZ_X RdZ_X V Vi eVc_R cVdZde c EYZd cVdZde c f deSV T __VTeVU SVeh VV_ eYV 72 DJ 4 D5 aZ_R_U Xc f _U 6bf ReZ _ TR_ SV f dVU e VdeZ ReV eYV WWbf V_Tj RU f decVdZde c

Typical Application (Boost)

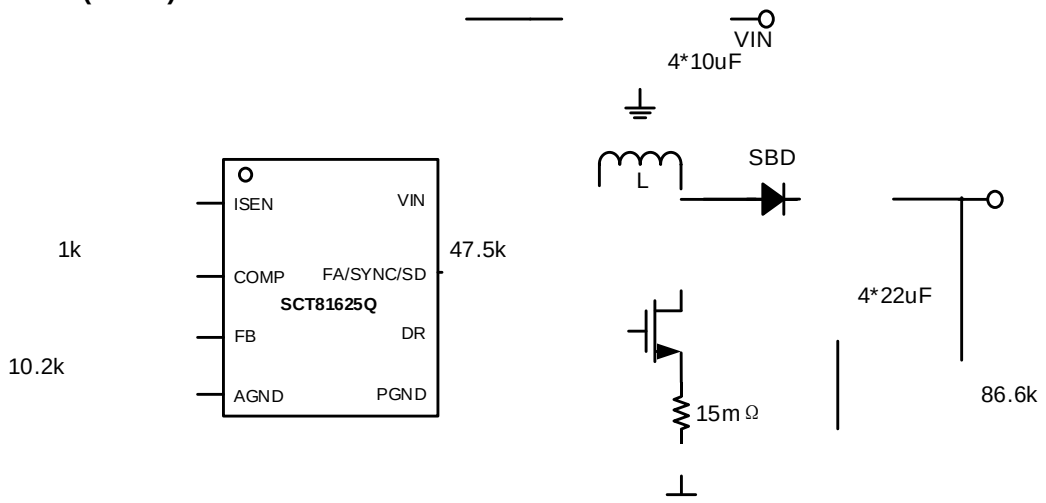


Figure 18. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Boost)

EYV aVdVc R_TV WZ_Uf Te cRWWTed eYV a h Vc df aa j d deVRUj deReV aVdReZ_ edR_dZV_e SVYRgZ c a deRSZZej R_U S deT _gVceVc VWWZV_Tj EYV Z_Uf Te cgR f V 54 cVdZdeR_TV R_U dRef dReZ_ Tf ccV_eZ_W V_TVd S eY VWWZV_Tj R_U eYV RX_Zf UV WeYV f eaf e g eRXV cZaa V =RcXVc Z_Uf TeR_TV gR f V cVUf TVd Z_Uf Te c Tf ccV_e cZaa V R_U eYVcVWcV VRUd e h Vc f eaf e g eRXV cZaa V 7 c R WZVU 54 cVdZdeR_TV R RcXVc gR f V Z_Uf Te c jZVUd YZXYVc VWWZV_Tj gZR cVUf TVU C> D R_U T cV ddVd 9 h VgVc R RcXVc Z_Uf Te ch ZeYZ_R XZgV_Z_Uf Te cWW Zj h Z XV_VdR j YRgV R XcVReVc dVcZVd cVdZdeR_TV eYVcVSj T f _eVdRTeZ_XeYZd VWWZV_Tj RUgR_eRXV

:_Uf Te cgR f Vd TR_YRgV cVgV_ & e VdR_TVh ZeY_ Tf ccV_eSZRd H YV_eYV Z_Uf Te cTf ccV_eRaac RTYVd dRef dReZ_ VgV Zed Z_Uf TeR_TV TR_UVTcVRdV e & Wd eYV gR f V Re 2 Tf ccV_e UVaV_UZ_X _Y h eYV Z_Uf Te cgV_U cUWZVd dRef dReZ_ H YV_dV VTeZ_XR_Z_Uf Te c TY dV Zed dReVU Tf ccV_e VdaVTZR j eYV dRef dReZ_ Tf ccV_e RcXVceYR_Zed aVR Tf ccV_eUf cZ_XeYV aVdReZ_

E TR Tf ReV eYV Tf ccV_eZ_eYV h cde TRdV f dV eYV Z_Z f Z_af eg eRXV Ri Z f f eaf eg eRXV Ri Z RU Tf ccV_eR_U Z_Z f dh ZeTYZ_X WWbf V_Tj WeYV Raa ZTReZ_ h YZV T _dZVcZ_XeYV Z_Uf TeR_TV h ZeY e VdR_TV R_U h a h VcT _gVcdZ_ VWWZV_Tj

7 cR S eT _gVceVc TR Tf ReV eYV Z_Uf Te c54 Tf ccV_eRd Z_6bf ReZ_ %

$$\frac{\qquad}{} \tag{14}$$

Where

- x V_{OUT} is the output voltage of the boost converter
- x I_{OUT} is the output current of the boost converter
- x V_{IN} is the input voltage of the boost converter
- x Zd eYV a h VcT _gVcdZ_ VWWZV_Tj

4R Tf ReV eYV Z_Uf Te cTf ccV_eaVR e aVR cZaa V :=AA Rd Z_6bf ReZ_ &

$$\frac{\qquad}{\qquad\quad\;\;} \tag{15}$$

Where

- x

TY dV_ Z_eYVdR_XV W 7e % 7 :WRgRfV h VceYR_ 7 ZdfdVU eYV_ac SV dh ZeYZ aVUR_TVZ_eVdRTeZ_d c dh ZeTYZ_X _ ZdV TR_ RWWTeeYV D4E) ' &B E Z ac gV aVdWc R_TV VdaVTZRj h ZeY GZ_ SV h) g ed ZeZd cVT V_UVUe fdVR Y cVdZde cReeYVZ_afee ac gZUVR_C4 WZeVc EYV cVdZde cZd aRTVUZ_dVcZVdh ZeYeYV G: aZ_h ZeY _j RSjaRddTRaRTZe cReeRTYVUe eYVG: aZ_UZdVTej 2 7 c 7TVdR ZdTRaRTZe cZd _VTVddRqj Z_eYZd T _WZfdReZ_ EYV Sf Z_afeTRaRTZe cR_UZ_Uf Te ch Z T __VTe _eYV eYVcdZUV WeYV cVdZde cReeYVZ_afe a h Vcdf aa j

Output Capacitor Selection

7 cd R feafeg eRXVcZaa V TY dVR h 6DC feafeTRaRTZe c ZVRTVdR ZdTRaRTZe c EjaZTR j ~% 7 TVdR ZdT feafeTRaRTZe cd h c Wc deRaaZTReZ_d 2 7 TVdR ZdT SjaRdd TRaRTZe cZd cVT V_UVUe SV aRTVURd T dVRd a ddZSVe eYV dh ZeTY _ UV 9ZXYVc TRaRTZe cgRfVd TR_SVfdVUe Z ac gVeYV RUeR_dZV_e cVda _dV 5fVe R TRaRTZe cd UVdReZ_X f _UVc 54 SZRd eYV SZRd TR_ dZX_ZdTR_ej cVUf TV TRaRTZR_TV 4VdR ZdT TRaRTZe cd TR_ dV de WeYVZc TRaRTZR_TV Re dReVUg eRXV EYVcVWcV VRgV RcXZ_ _eYV g eRXV dReZ_Xe V_dfcV RUVbfReV VWWTegV TRaRTZR_TV 7c eYV cVbfZdVU feafeg eRXV cZaa V fdVeYV VbfReZ_) R_U * e TRTf ReVeYV Z_Z f cVbfZdVU VWWTegV TRaRTZR_TV 4 FE

(18)

(19)

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Power MOSFET Selection

EYV W hZX aRdR VeVcd dY f U SV eR V_ Z_e T _dZUVdReZ_ Wc > D76E+ eYV _cVdZdeR_TV C5DP eYV Z_Z f XReVeYcVdY Ug eRXVGE9P>: eYVe eR XReV TYRcXV B X eYV cVgVcdVeaR_dWc TRaRTZR_TV 4CDD R_U eYV RiZ f UdRZ_e d fcTVg eRXVGBP>2I EYV aVR dh ZeTYZ_Xg eRXV SVeh VV_UdRZ_e d fcTV Z_R3 deZd XZgV_Sj

$$V_{SW\_PEAK} \quad V_{IN} \quad V_D \tag{20}$$

EYV_eYVGBP>2I Wa h Vc> D76E dY f U SV XcVReVceYR_eYV aVR dh ZeTYZ_Xg eRXV

EYV aVR dh ZeTYZ_X Tf ccV_eWh Z_XeYc f XYeYV > D76E ZdXZgV_Sj +

$$I_{Q\_PEAK} \quad I_{LPEAK} \tag{21}$$

EYV C> D Tf ccV_eeYc f XYeYV > D76E ZdTR Tf ReVU Sj +

$$I_{Q\_RMS} \quad \sqrt{(I_{LDC}{}^2 \quad \frac{I_{LPP}}{12})} * D \tag{22}$$

EYV_a h VcUZddZaReZ_Z_> D76E TR_SV VdeZ ReVU Sj +

$$P_{DIS} \quad I_{Q\_RMS}^2 \; uR_{DS\_ON} \; uD_{MAX} \quad V_O \quad V_{IN\_MIN} \quad Iu_{Q\_PEAK} \quad \frac{Q_g \; uf_{SW}}{I_G} \tag{23}$$

Where

I_G is the gate drive current.

EYVe eR a h VcUZddZaReZ_ W> D76E Z_TfUVd T _UfTeZ_ dd Rd dY h _ Z_eYV WZdeeVc R_U dh ZeTYZ_X dd Rd dY h _ Z_eYV dVT _UeVc EYVe eR a h VcUZddZaReZ_dY f U SVh ZeYZ_aRT RXVeYVc R cYV dV V

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

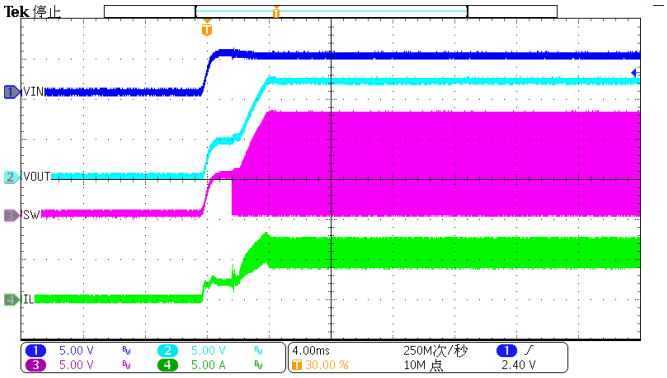


Figure 19. Power up(Iload=2A)

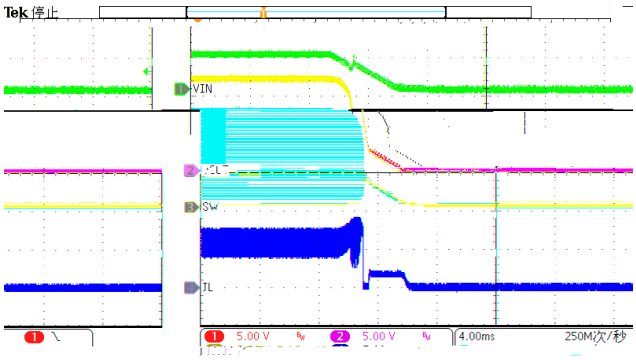


Figure 20. Power down(Iload=2A)

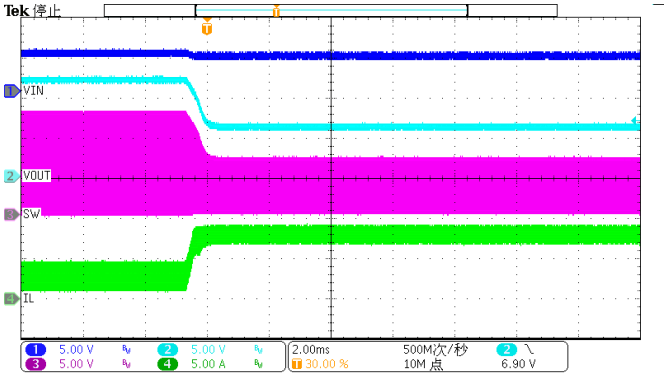


Figure 21. Over current protection (Iload=5A)

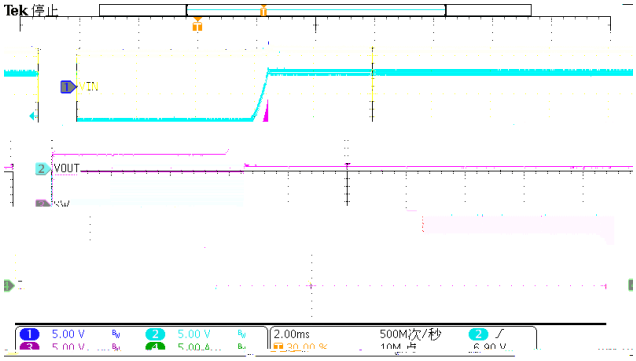


Figure 22. Over current recovery (Iload=5A)

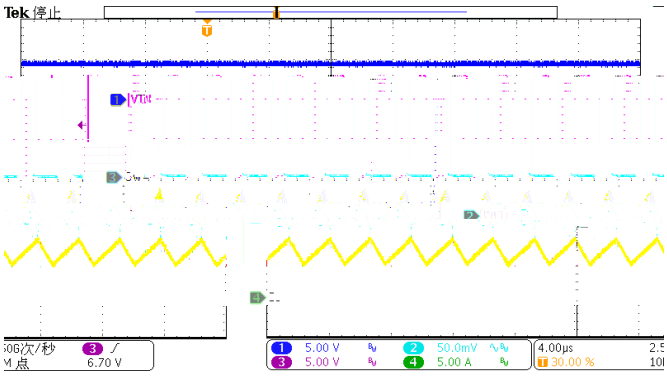


Figure 23. Steady-state (Iload=2A)

Figure 24. Sync Frequency

Typical Application (Sepic)

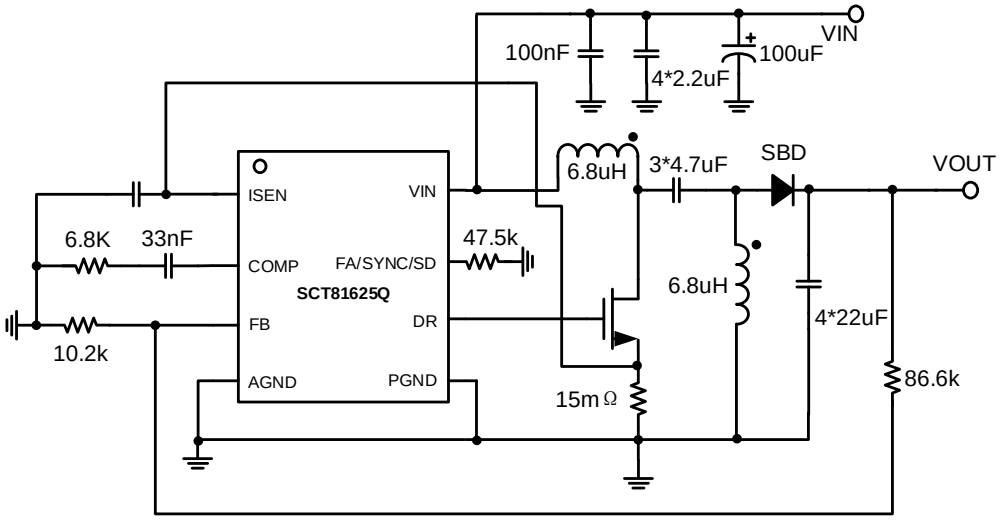


Figure 25. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Sepic)

2 X U df V Wc UVeVc Z_Z_X eYV Z_Uf TdR_TV e f dV Y _U V

EYVe eR a h VcUZddZaReZ_ W> D76E Z_TfUVd T _UfTeZ_ dd Rd dY h _Z_eYVWddeeVc R_U dh ZeTYZ_X dd Rd dY h _Z_eYVdVT _UeVc EYVe eR a h VcUZddZaReZ_dY f USVh ZeYZ_aRT RXVeYVc R dReZ_Xd

Output Diode Selection

EYVUZUVReeYV feafedZUV fdeh ZeYdeR_UeYVcVgVcdVg eRXVh YV_eYV> D76E Zdefc_VU _EYVaVR cVgVcdV g eRXVZdXgV_Sj+

$$V_{D\_PEAK} \quad V_{IN\_MAX} \quad V_{O\_MAX} \tag{35}$$

EYVUZUVdY fURd SVTRaRSVe Wh dh ZeTYaVR TfccV_e:BPA62<

EYVa h VcUZddZaReZ_ WeYVUZUVZdVbfRe eYVWdhRdUg eRXVUca feZaZVd feafeTfccV_e DTYeej UZUVd RcVcVT V_UVUYVcVe Z_Z ZVeYVa h Vc dd

Coupling Capacitor Selection

7 cTVdR ZdTTRaRTZe cdh ZeY h 6DC eYVaVR e aVR g eRXVcZaaV _T fa Z_XTRaRTZe cZdVdeZ ReVUSj+

$$V_{CS}' \quad \frac{I_O \ u D_{MAX}}{C_S \ u f_{SW}} \tag{36}$$

EYV RiZf g eRXVRTc ddeYV Tfa Z_XTRaRTZe cZd RiZf Z_afeg eRXV EYVg eRXVcReZ_X WeYV Tfa Z_X TRaRTZe c fdeSVXcVReVceYR_Ze

EYVC> D TfccV_e WT fa Z_XTRaRTZe cZdXgV_Sj+

$$I_{CS\_RMS} \quad I_O \quad \sqrt{\frac{V_O \ u V_D}{V_{IN\_MIN}}} \tag{37}$$

EYVcVZd R RcXVC> D TfccV_eeYc fXY Tfa Z_XTRaRTZe ccVReZgVe feafea h Vc 6_dfcVeYV Tfa Z_XTRaRTZe c TR_hZeYdeR_UZeh ZeYX UYVReXV_VcReZ_e YRgVac aVceYVc R aVdWc R_TV

Input Capacitor Selection

EYVD6A:4 YRdR_Z_UfTe cReZ_afedZUVeYfdeYVZ_afeTfccV_eZdT _eZ_f fdR_UecZR_Xf RcEYVC> D TfccV_eWh Z_X eYc fXYeYVZ_afeTRaRTZe cZdXgV_Sj+

$$I_{IN\_RMS} \quad \frac{'I_{L1}}{\sqrt{12}} \tag{38}$$

DZ_TVZ_afeTfccV_ecZaaVZdcVReZgV h eYVTRaRTZR_TVh fUSV_ee TcZdTR HYZV 7Z_eeR cYZXYVc gRfVZddec _Xj cVT V_UVUZ_ dUVce acgZUVdeRSVZ_afedfaaj

Output Capacitor Selection

DZ ZRce S deT _gVceVc eYVD6A:4 feafeTRaRTZe cdfWWcd RcXVTfccV_ecZaaV EYVTRaRTZR_TV fdeSVV_ fXY e acgZUVeYV RUTfccV_e EYV RiZf g eRXVcZaaVZ_eYV feafeTRaRTZe cZd+

$$'V_{OUT} \quad \frac{I_O \ u D_{MAX}}{C_{OUT} \ u f_{SW}} \quad ESR \ u \ I_{L1\_PEAK} \quad I_{L2\_PEAK} \tag{39}$$

2ddf Z_XTVdR ZdTTRaRTZe cdRcVfdVUYVcVR_U6DC TR_SVZX_ cVU eYV feafeTRaRTZe cZdXgV_Sj+

$$C_{OUT} \ t \frac{I_O \ u D_{MAX}}{V_{OUT}' \quad f_{SW}} \tag{40}$$

EYV feafeTRaRTZe c fdeYRgVRV_ fXYC> D TfccV_edReZ_Xe YR_UVeYV RiZf C> D TfccV_eZ_eYV feafe TRaRTZe c TRTf ReVUSj+

$$I_{COUT\_RMS} \quad I_O \quad \sqrt{\frac{D_{MAX}}{1 \quad D_{MAX}}} \qquad (41)$$

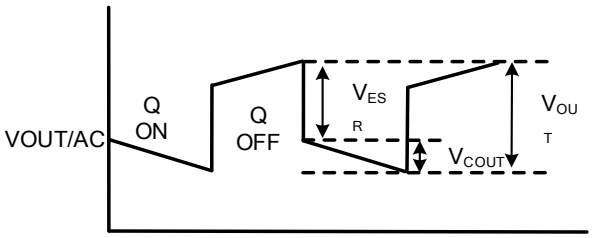


Figure 26. Output Voltage Ripple